

USPTO Serial No.: 10/767,384
Fatemizadeh et al.
Response to Office Action mailed August 24, 2005

Amendment to the Claims:

1. (Original) A method of forming a semiconductor device, comprising:
 - providing a substrate;
 - forming a first layer of semiconductor material over the substrate;
 - removing a portion of the first layer to provide a layer offset between a removed portion of the first layer and a remaining portion of the first layer;
 - forming an oxide layer of uniform thickness over the removed portion of the first layer and the remaining portion of the first layer;
 - planarizing the oxide layer so that the oxide layer over the remaining portion of the first layer is removed;
 - forming a polysilicon region over the planarized oxide layer;
 - forming an epi region over the remaining portion of the first layer;
 - forming a trench between the polysilicon region and the epi region extending vertically down to the oxide layer; and
 - depositing oxide in the trench down to the oxide layer to isolate the polysilicon region.
2. (Original) The method of claim 1, wherein the substrate is N-type semiconductor material.
3. (Original) The method of claim 1, wherein the first layer of semiconductor material receives N-type dopants.

USPTO Serial No.: 10/767,384

Fatemizadeh et al.

Response to Office Action mailed August 24, 2005

4. (Original) The method of claim 1, wherein the step of removing a portion of the first layer includes the step of removing the first layer substantially down to the substrate.

5. (Original) The method of claim 1, further including the steps of:

- forming a first well in the polysilicon region;
- forming a second well in the first well;
- forming a first transistor in the first well; and
- forming a second transistor in the second well.

6. (Original) The method of claim 5, further including the steps of: forming a third well in the epi region; and forming a power transistor in the third well.

7. (Cancelled)

8. (Currently Amended) ~~The method of claim 7, further including the steps of:~~ A method of forming an integrated circuit having a driver device in proximity to a power device, comprising:

- forming an oxide layer below the driver device;
- forming a trench between the driver device and the power device, wherein the trench extends down to the oxide layer;
- depositing oxide in the trench down to the oxide layer to isolate the driver device from the power device;
- providing a substrate;
- forming a first layer of semiconductor material over the substrate;
- removing a portion of the first layer to provide a layer

USPTO Serial No.: 10/767,384

Fatemizadeh et al.

Response to Office Action mailed August 24, 2005

offset between a removed portion of the first layer and a remaining portion of the first layer; and

forming the oxide layer having uniform thickness over the removed portion of the first layer and the remaining portion of the first layer.

9. (Original) The method of claim 8, further including the steps of:

planarizing the oxide layer so that the oxide layer over the remaining portion of the first layer is removed;

forming a polysilicon region over the planarized oxide layer;

forming an epi region over the remaining portion of the first layer; and

forming the trench between the polysilicon region and the epi region extending vertically down to the oxide layer.

10. (Original) The method of claim 9, wherein the first layer of semiconductor material is an extension layer of the substrate.

11. (Original) The method of claim 9, wherein the first layer of semiconductor material is an epi layer.

12. (Original) The method of claim 9, further including the steps of:

forming a first well in the polysilicon region;

forming a second well in the first well;

forming a first transistor in the first well; and

forming a second transistor in the second well.

USPTO Serial No.: 10/767,384

Fatemizadeh et al.

Response to Office Action mailed August 24, 2005

13. (Original) The method of claim 12, further including the steps of: forming a third well in the epi region; and forming a power transistor in the well.

14. (Cancelled)

15. (Currently amended) ~~The semiconductor device of claim 14, wherein the process further includes the steps of: A~~
semiconductor device having a driver device in proximity to a power device, the semiconductor device being made by the process comprising the steps of:

forming an oxide layer below the driver device;

forming a trench between the driver device and the power device, wherein the trench extends down to the oxide layer;

depositing oxide in the trench down to the oxide layer to isolate the driver device from the power device;

providing a substrate;

forming a first layer of semiconductor material over the substrate;

removing a portion of the first layer to provide a layer offset between a removed portion of the first layer and a remaining portion of the first layer; and

forming the oxide layer having uniform thickness over the removed portion of the first layer and the remaining portion of the first layer.

16. (Original) The semiconductor device of claim 15, wherein the process further includes the steps of:

planarizing the oxide layer so that the oxide layer over the remaining portion of the first layer is removed;

USPTO Serial No.: 10/767,384

Fatemizadeh et al.

Response to Office Action mailed August 24, 2005

forming a polysilicon region over the planarized oxide layer;

forming an epi region over the remaining portion of the first layer; and

forming the trench between the polysilicon region and the epi region extending vertically down to the oxide layer.

17. (Cancelled)

18. (Currently amended) ~~The method of claim 17, further including the steps of:~~ A method of forming a first semiconductor device in proximity to a second semiconductor device on an integrated circuit, comprising:

forming an oxide layer below the first semiconductor device;

forming a trench between the first and second semiconductor devices, wherein the trench extends down to the oxide layer;

depositing oxide in the trench down to the oxide layer to isolate the first and second semiconductor devices;

providing a substrate;

forming a first layer of semiconductor material over the substrate;

removing a portion of the first layer to provide a layer offset between a removed portion of the first layer and a remaining portion of the first layer; and

forming the oxide layer having uniform thickness over the removed portion of the first layer and the remaining portion of the first layer.

19. (Original) The method of claim 18, further including the steps of:

USPTO Serial No.: 10/767,384

Fatemizadeh et al.

Response to Office Action mailed August 24, 2005

planarizing the oxide layer so that the oxide layer over the remaining portion of the first layer is removed;

forming a polysilicon region over the planarized oxide layer;

forming an epi region over the remaining portion of the first layer; and

forming the trench between the polysilicon region and the epi region extending vertically down to the oxide layer.

20-24. (Cancelled)